What is claimed is:

1. An apparatus for scrambling and descrambling data in an optical disk system, the apparatus comprising:

a shift register which is initialized at a predetermined initial value and which generates 16 bits of a scrambling word at a time using a predetermined parallel operation; and

an XOR logic operator which performs an XOR logic operation on the scrambling word and every bit of scrambled data or descrambled data corresponding to the scrambling word.

2. The apparatus of claim 1, wherein the shift register is a 15-bit shift register.

3. The apparatus of claim 2, wherein the shift register performs an XOR logic operation on a seventh bit and a fifteenth bit, on a first bit, an eighth bit, and a twelfth bit, on a second bit, a ninth bit, and a thirteenth bit, on a third bit, a tenth bit, and a fourteenth bit, on a fourth bit, an eleventh bit, and a fifteenth bit, on the first bit and a fifth bit, on the second bit and a sixth bit, on a third bit and the seventh bit, on the fourth bit and the eighth bit, on the fifth bit and the ninth bit, on the sixth bit and the tenth bit, on the seventh bit and the eleventh bit, on the eighth bit and the twelfth bit, on the ninth bit and the thirteenth bit, and on the tenth bit and the fourteenth bit, and stores the results of the XOR logic operations in the first through fifteenth bits, respectively.

4. The apparatus of claim 3, wherein 8 upper bits of the scrambling word are the first through eighth bits of the shift register, and 8 lower bits of the scrambling word are the results of the XOR logic operations performed on the fourth bit and the eighth bit, on the fifth bit and the ninth bit, on the sixth bit and the tenth bit, on the seventh bit and the eleventh bit, on the eighth bit and the twelfth bit, on the ninth bit and the thirteenth bit, on the tenth bit and the fourteenth bit, and on the eleventh bit and the fifteenth bit.

5. The apparatus of claim 1, wherein 16 bits of the scrambled data or the descrambled data are read from a memory in the optical disk system in parallel at a time.

6. An apparatus for generating a scrambling word used to scramble and descramble data in an optical disk system, the apparatus comprising:

a bit storing means which stores at least 15 bits; and

a calculating means which calculates first through fifteenth bits of the bit storing means in parallel during one clock cycle and inputs the results of the calculation back into the bit storing means,

wherein the calculating means performs an XOR logic operation on a seventh bit and a fifteenth bit, on a first bit, an eighth bit, and a twelfth bit, on a second bit, a ninth bit, and a thirteenth bit, on a third bit, a tenth bit, and a fourteenth bit, on a fourth bit, an eleventh bit, and a fifteenth bit, on the first bit and a fifth bit, on the second bit and a sixth bit, on a third bit and the seventh bit, on the fourth bit and the eighth bit, on the fifth bit and the ninth bit, on the sixth bit and the tenth bit, on the seventh bit and the eleventh bit, on the eighth bit and the twelfth bit, on the ninth bit and the thirteenth bit, and on the tenth bit and the fourteenth bit, and inputs the results of the XOR logic operations into the bit storing means.

7. The apparatus of claim 6, wherein 8 upper bits of the scrambling word are the first through eighth bits of the bit storing means, and 8 lower bits of the scrambling word are the results of the XOR logic operations performed on the fourth bit and the eighth bit, on the fifth bit and the ninth bit, on the sixth bit and the tenth bit, on the seventh bit and the eleventh bit, on the eight bit and the twelfth bit, on the ninth bit and the thirteenth bit, on the tenth bit and the fourteenth bit, and on the eleventh bit and the fifteenth bit.

8. A method for scrambling and descrambling data in an optical disk system, the method comprising:

(a) generating a predetermined scrambling word; and

(b) performing an XOR logic operation on the scrambling word and scrambled data or descrambled data,

wherein the scrambling word comprises 16 bits and is generated through a parallel operation performed using a shift register.

9. The method of claim 8, wherein the shift register is a 15-bit shift register.

10. The method of claim 9, wherein step (a) comprises performing an XOR logic operation on a seventh bit and a fifteenth bit, on a first bit, an eighth bit, and a twelfth bit, on a second bit, a ninth bit, and a thirteenth bit, on a third bit, a tenth bit, and a fourteenth bit, on a fourth bit, an eleventh bit, and a fifteenth bit, on the first bit and a fifth bit, on the second bit and a sixth bit, on a third bit and the seventh bit, on the fourth bit and the eighth bit, on the fifth bit and the ninth bit, on the sixth bit and the tenth bit, on the seventh bit and the eleventh bit, on the eighth bit and the twelfth bit, on the ninth bit and the thirteenth bit, and on the tenth bit and the fourteenth bit, and storing the results of the XOR logic operations in the first through fifteenth bits, respectively.

11. The method of claim 10, wherein step (a) comprises:

generating the first through eighth bits of the shift register as 8 upper bits of the scrambling word; and

generating the results of the XOR logic operations performed on the fourth bit and the eight bit, on the fifth bit and the ninth bit, on the sixth bit and the tenth bit, on the seventh bit and the eleventh bit, on the eight bit and the twelfth bit, on the ninth bit and the thirteenth bit, on the tenth bit and the fourteenth bit, and on the eleventh bit and the fifteenth bit as 8 lower bits of the scrambling word.